REMARKS

The above Amendments and these Remarks are being submitted in response to the Office Action dated August 14, 2002.

I. Summary of the Examiner's Rejections

Claims 1-6, 8, 9, 11, 18, 41 and 49 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1-6, 8-9, 15-18, 20-21, 41, 43-47, 49 and 53-54 stand rejected under 35 U.S.C. §102(b) as being anticipated by Fallon, et al. (U.S. Patent No. 5,872,051). Claims 11 and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Fallon, et al. in view of Takano, et al. (U.S. Patent No. 6,376,907). Claims 7, 13, 19, 25 and 42 have been withdrawn from consideration by the Examiner.

II. Summary of the Applicants' Amendments

The specification has been amended to correct minor typographical and grammatical errors present therein. The Applicants respectfully submit that no new matter has been added by such amendments. Claims 21 and 41-42 have been cancelled. Claims 1, 5, 9, 15 and 17-18 have been amended.

III. Applicants' Response to the Examiner's Rejections

The Applicants traverse the rejection of the claims as described above for the reasons set forth in greater detail below.

A. Withdrawal of claims 7 and 19

The Applicants traverse the withdrawal of claims 7 and 19 from consideration as "...flip-chip attachment..." as recited in each of the aforementioned claims does in fact read on FIG. 5. The Examiner's attention is directed, for example, to page 5, lines 2-5 of the originally filed specification which provides support for how packaged and unpackaged semiconductor die are connected within the claimed device. Included within the specification is flip-chip attachment. Thus, as the originally filed specification and figures provide support for "... flip-chip attachment..." as recited in claims 7 and 19, the Applicants submit that such claims do read on the embodiment illustrated in FIG. 5, and that the withdrawal of claims 7 and 19 is improper. Accordingly, reconsideration of the withdrawal of claims 7 and 19 from consideration is respectfully requested.

B. Rejection of claims under 35 U.S.C. §112

(i) Claim 1

Claim 1 has been amended to further define the novel structural aspects that the Applicants regard as the invention. Accordingly, reconsideration of the rejection of claim 1 is respectfully requested.

(ii) Claim 18

Claim 18 has been amended to further define the attachment between the graphics processing die and the package module according to the present invention. Accordingly, reconsideration of the rejection of claim 18 is respectfully requested.

(iii) Claim 49

The Applicants traverse the Examiner's statement on page 3, paragraph 4 of the Office Action which states in pertinent part "...The term 'substantially' is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention..." as ample support for ascertaining the degree provided by the term substantially can be found, for example, in FIG. 1 and FIG. 5 of the instant application which illustrates the semiconductor die being encapsulated in a structure having a substantially rectangular shape or footprint. Thus, as the figures provide a clear illustration of the claimed structure, the Applicants submit that there is support in the originally filed application for ascertaining the degree of the term substantially as recited in claim 49. Accordingly, reconsideration of the rejection of claim 49 is respectfully requested.

C. Rejection of claims under 35 U.S.C. §102

(i) Claims 1-9 and 11

Claim 1 has been amended to further define the structural configuration of the present invention. Support for the defined structure can be found, for example, in FIG. 1 of the originally filed drawings. More specifically, claim 1 includes the following structural limitation which is not disclosed in Fallon et al:

> "...an unpackaged semiconductor die directly attached to the package module, the unpackaged semiconductor die encapsulated onto the package module in a structure having a substantially rectangular footprint..."

Consequently, Fallon et al. does not anticipate the invention as defined in claim 1. As understood, Fallon et al. discloses and illustrates a module structure where "...the wire bond chip, bond wires and coupling pads are encapsulated with an organic material..." (see, for example, FIG. 46 and col. 37, lines 63-64). However, FIG. 46 does not illustrate and the corresponding portion of the specification do not describe, for example, the wire bond chip as being encapsulated within a structure having a substantially rectangular footprint. In fact, no encapsulation structure is illustrated in FIG. 46. Additionally, the wire bond chip does not appear to be "...directly attached..." to the underlying substrate as defined in claim 1, as the wire bond chip is actually attached to a metal pad structure (710). Accordingly, as the aforementioned structural limitation of claim 1 is not disclosed within Fallon et al., the Applicants submit that Fallon et al. does not anticipate the invention as defined in claim 1. Accordingly, reconsideration of the rejection of claim 1 is respectfully requested.

Claims 2-9 and 11 directly or indirectly depend upon and include all the limitations of claim 1 and are allowable at least for the reasons set forth above with respect to claim 1. Accordingly, reconsideration of the rejection of claims 1-9 and 11 is respectfully requested.

(ii) Claims 15-21 and 23

Claim 15 is an apparatus claim directed to a device including, among other things:

> "...a graphics-processing die directly attached to the package module, the graphics-processing die encapsulated on the package module in a structure having a rectangular footprint...."

As such, claim 15, like claim 1 above, includes a structural limitation defining the graphics-processing die being "...encapsulated on the package module in a structure having a rectangular footprint...." As such, claim 15 is allowable at least for the reasons set forth above with respect to claim 1. Accordingly, reconsideration of the rejection of claim 15 is respectfully requested.

Claims 16-21 and 23 directly or indirectly depend upon and include all the limitations of claim 15 and are allowable at least for the reasons set forth above with respect to claim 15. Accordingly, reconsideration of the rejection of claims 16-21 and 23 is respectfully requested.

(iii) Claims 43-47, 49 and 53-54

Claim 43 is directed to a multi-die module having the following structure:

"...an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a rectangular footprint...."

As such, claim 43, like claim 1 above, defines a device having a structure where an "...unpackaged semiconductor die..." is both "...mounted to the first surface of the substrate..." and "...encapsulated in a structure having a rectangular footprint...." Thus, claim 43 is submitted to be allowable at least for the reasons set forth above with respect to claim 1. Accordingly, reconsideration of the rejection of claim 43 is respectfully requested.

Claims 44-47, 49 and 53-54 directly or directly depend upon and include all the limitation of claim 43 and are allowable at least for the reasons set forth above with respect to claim 43. Accordingly, reconsideration of the rejection of claims 43-47, 49 and 53-54 is respectfully requested.

D. Rejection of claims under 35 U.S.C. §103

(i) Claim 11

Claim 11 depends upon and includes all the limitations of claim 1 and is submitted to be allowable at least for the reasons set forth above with respect to claim 1. Additionally, adding the teachings of Takano et al. to the teachings of Fallon et al. will also not render this claim obvious as Takano et al. does not overcome the aforementioned shortcomings associated with Fallon et al. More specifically, Takano et al. does not teach or suggest a device having a structure or configuration including "...an unpackaged semiconductor die directly attached to the package module, the unpackaged semiconductor die encapsulated onto the package module in a structure having a substantially rectangular footprint..." as Takano et al. does not disclose a device having such structure. As understood, Takano et al. is directed to a ball grid array (BGA) type package for a semiconductor device including a cover plate having a plurality of discontinuous bonding portions (see, for example, column 6, lines 33-37), for protecting and dissipating heat produced by the underlying device. However, as discussed above, the aforementioned limitation regarding the unpackaged semiconductor die being encapsulated onto the substrate in a structure having a rectangular footprint is not disclosed within Takano et al. Accordingly, as neither Fallon et al. nor Takano et al. teach or suggest the aforementioned structural limitation, the combination of such references does not render the invention as defined in claim 1 obvious. As claim 11 depends upon and includes all the

limitations of claim 1, claim 11 is also not rendered obvious by the combination of Fallon et al. and Takano et al. Accordingly, reconsideration of the rejection of claim 11 is respectfully requested.

(ii) Claim 23

Claim 23 depends upon and includes all the limitations of claim 15 and is submitted to be allowable at least for the reasons set forth above with respect to claim 15. In addition, adding the teachings of Takano et al. to the teachings of Fallon et al. also does not render this claim obvious as Takano et al. does not disclose a device including "...a graphics-processing die directly attached to the package module, the graphics-processing die encapsulated on the package module in a structure having a rectangular footprint...." As understood, Takano et al. is directed to a BGA package for a semiconductor device including a cover plate having a plurality of discontinuous bonding portions (see column 6, lines 33-37), for protecting and dissipating heat produced by the underlying device. No discussion of a graphics-processing die, or any corresponding device, being encapsulated on a substrate or package module in a substantially regular structure is present in Takano et al.

Thus, as neither Fallon et al. nor Takano et al. teach or suggest the aforementioned structural limitation of claim 15, the combination of such references does not render the invention as defined in claim 15 obvious. As claim 23 depends upon and includes all the limitations of claim 15, the Applicants submit that claim 23 is also not rendered obvious by the combination of Fallon et al. and. Takano et al. Accordingly, reconsideration of the rejection of claim 23 is respectfully requested.

Based on the above amendments and remarks, the Applicants submit that claims 1-9, 11, 15-20, 23, 43-47, 49 and 53-54 are now in proper condition for allowance and such action is earnestly solicited.

The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-0441 for any payment in connection with this communication, including any fees for extension of time, which may be required. The Examiner is invited to call the undersigned if such action might expedite the prosecution of this application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the paragraph beginning on page 3, line 22, with the following:

In the embodiment illustrated, package module 100 has unpackaged die 110 mounted on it, as well as packaged die 120 and 130. In at least one embodiment, unpackaged die 110 is a data processor, such as a general purpose processor or a graphics processor, and packaged die 120 and 130 are memory packaged in chip Scale Packages (CSP) or stacked CSP memories. In other embodiments, unpackaged die 110 may be an additional processor such as an audio processor, a general purpose processor, a controller, etc., while packaged die 120 and 130 may be static random access memories (SRAM), dynamic random access memories (DRAM), read only memories (ROM), flash memories, electrically erasable programmable memories (EEPROMS), or any other suitable memory type of combination of types. In addition, packaged die 120 and 130 may be processors of the same or a different type than unpackaged die 110. Various embodiments of the present invention may employ different combinations of [packaged] unpackaged semiconductor die 110 and [unpackaged] packaged semiconductor die 120 and 130, including the use of two unpackaged semiconductor die 110 and only one packaged semiconductor die 120, or multiple packaged semiconductor die 120 and 130 with no unpackaged semiconductor die 110.

Please replace the paragraph beginning on page 4, line 6 with the following:

FIG. 2 illustrates a partially completed multi-die module. Multi-die module substrate 140 is shown with unpackaged semiconductor die 110 attached in preparation for wire bonding. In one embodiment, multi-die module substrate 140 is [buildup] a built up substrate having four to six layers. In another embodiment, multi-die module substrate 140 is a Bizmalemide Triazine (BT) substrate having two to six layers. It will be appreciated that any suitable substrate may be employed according to the teachings set forth herein.

Please replace the paragraph beginning on page 4, line 12 with the following:

FIG. 3 illustrates the partially completed multi-die module of FIG. 2, but now [wire] bond wires 175 have been added to make an electrical connection between multi-die module substrate 140 and unpackaged semiconductor die 110. In at least one embodiment, bond wires

175 are made of a corrosion resistant material, such as gold, to resist corrosion, but other suitable wire types or similar means of electrical connection may be employed as desired.

Please replace the paragraph beginning on page 6, line 1 with the following:

FIG. 8 illustrates another method of insulating electrical connections between unpackaged semiconductor die 111 and multi-die module substrate 140. Since all of the electrical connections are underneath unpackaged semiconductor die 111, there is no need for total encapsulation of unpackaged semiconductor die 111 to protect the electrical connections. Consequently, unpackaged semiconductor die 111 is underfilled with underfill material 170. Underfill material 170 may include, but is not limited to, ASEUA03 and ASEUA04 types of underfill materials.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 21 and 41-42 and amend claims 1, 5, 9, 15 and 17-18 to read as shown below by substituting the claim(s) below for claims having the same number as follows.

1. (Amended) A device comprising:

a package module including a substrate having a standard package footprint [size based on a standard package];

an unpackaged semiconductor die directly attached to the package module, the unpackaged semiconductor die encapsulated onto the package module in a structure having a substantially rectangular footprint; and

a packaged semiconductor die attached to the [multi-die] package module.

5. (Amended) The device as in claim 1, wherein a plurality of packaged semiconductors are attached to the [multi-die] package module.

9. (Twice Amended) The device as in claim 1, wherein the [unpackaged semiconductor die is] encapsulated [onto the package module] structure has a footprint greater than the footprint of the unpackaged semiconductor die.

15. (Amended) A device comprising:

a package module sized to be interchangeable with standard package sizes;

a graphics-processing die directly attached to the package module, the graphics - processing die encapsulated on the package module in a structure having a rectangular footprint; and

a packaged memory die attached to the package module.

17. (Amended) The device as in claim 15, wherein a plurality of packaged memory are attached to the [multi-die] package module.

18. (Amended) The device as in claim 15, wherein directly attached includes the graphics processing die being wire bonded to the package module.